InGaAs/InAlAs/AlAs Heterostructure Barrier Varactors for Harmonic Multiplication

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***Abstract*—In this letter, we report on the radio frequency (RF) characterization up to 110 GHz of probeable high-performance heterostructure barrier varactors fabricated from InP-based strained epilayers. By making use of a dual step-like barrier scheme, the voltage handling is as high as 12 V whereas the capacitance ratio at 85 GHz achieves 5 : 1 for a zero-bias capacitance of 1 fF/μm^2 without deviation in the frequency band investigated. Good agreement between calculated and measured scattering parameters is found on the basis of electromagnetic simulation of diode embedding.**

***Index Terms*—Harmonic multiplier, heterostructure, varactor.**

I. Introduction

HETEROSTRUCTURE barrier varactor with natural symmetrical *CV* characteristics about zero bias have been recently proposed [1]. They make use of an heterostructure potential barrier to prevent conduction through the device and thus allow voltage-dependent depletion region to develop in the cladding layers. Such a special symmetry with unbiased devices makes them attractive to up-convert power with only odd-harmonics at millimeter and submillimeter wavelengths by reactive nonlinearity. The standard Schottky varactor also exhibits such a symmetry in a back-to-back configuration but suffers from self-biasing effects [2]. For the design of multiplier block, the knowledge of the device scattering parameters is of prime importance to calculate the optimum source and load impedances through harmonic balance simulations and to synthesize them through matching circuits. In this letter, we report on extensive radio frequency (RF) measurements in a broad frequency band of heterostructure barrier varactors (HBV's) fabricated from high-quality InP-based heterojunctions. To this aim, two kinds of test configurations have been fabricated: 1) a coaxial-type directly probeable pattern which permits us to measure the intrinsic voltage-dependent lumped elements without deembedding techniques and 2) a coplanar waveguide (CPW)-type probing pattern from which the extrinsic reactive elements due to access and interconnecting sections can be assessed.

II. Coaxial- and CPW-Type Technology

Fig. 1 shows scanning electron micrographs of the test patterns mentioned in Section I. The coaxial-type test pattern consists of a mesa etched circular-shaped diode with a concentric ring-shaped side contact. The RF probes are positioned directly onto the middle and side ohmic contacts for dc and RF contacting the devices. Not expected at first glance, it was found that such a probing technology, easily implemented, works efficiently and accurately up to 110 GHz as seen in the following. In counterpart, there are minimum requirements for the diode diameter (about 15 μm) and electrode interdistance (10 μm) below which contacting a device becomes too troublesome. The second maskset makes use of a conventional CPW configuration. Here, this microwave-compatible technology permits us to characterize small area device interconnected to the hot CPW line by means of air bridge and deep etch techniques. On the other hand, by mixing the experimental data achieved from the first test technology and those from the CPW configuration, the device in its environment can be fully characterized.

The epitaxial material grown by gas source molecular beam epitaxy, was similar to that reported in [3] a dual barrier configuration. In short, the blocking layer consists of an $In_{0.52}Al_{0.48}As$ 5-nm-thick/AlAs 3-nm-thick/$In_{0.52}Al_{0.48}As$ 5-nm-thick trilayered heterostructure. This blocking layer was sandwiched between two 300-nm-thick cladding layers whose doping concentrations were either 1×10^{17} cm^{-3} or twice higher depending on the targeted tripler application. In addition, thick (0.5–1 μm) capping and buried layers are grown for implementing low-resistance contact regions. The test samples were fabricated using the technological procedures reported in [3].

III. RF Measurements

Fig. 2 shows the capacitance-voltage characteristic of a 25-μm-diameter coaxial-type device measured at 500 MHz and 85 GHz, respectively. The doping level of the device under test is $N_d = 1 \times 10^{17}$ cm^{-3} and the measured breakdown voltage is 12 V in that case. The zero-bias capacitance is 420 fF corresponding to a relative capacitance of about 1 fF/μm^2. Such a low capacitance level is a direct consequence of the epitaxial stacking of two diodes in series. The capacitance ratio achieves 5 : 1. Also interesting is the invariance of these characteristics upon frequency reflecting the high quality of the epilayers. In contrast, this result does not presume of carrier velocity saturation effects [4], [5] which are solely revealed under large-signal conditions.

Fig. 3 shows the frequency dependence of the imaginary part of the admittance of a device in CPW technology measured by means of two Hewlett Packard (HP) network an-

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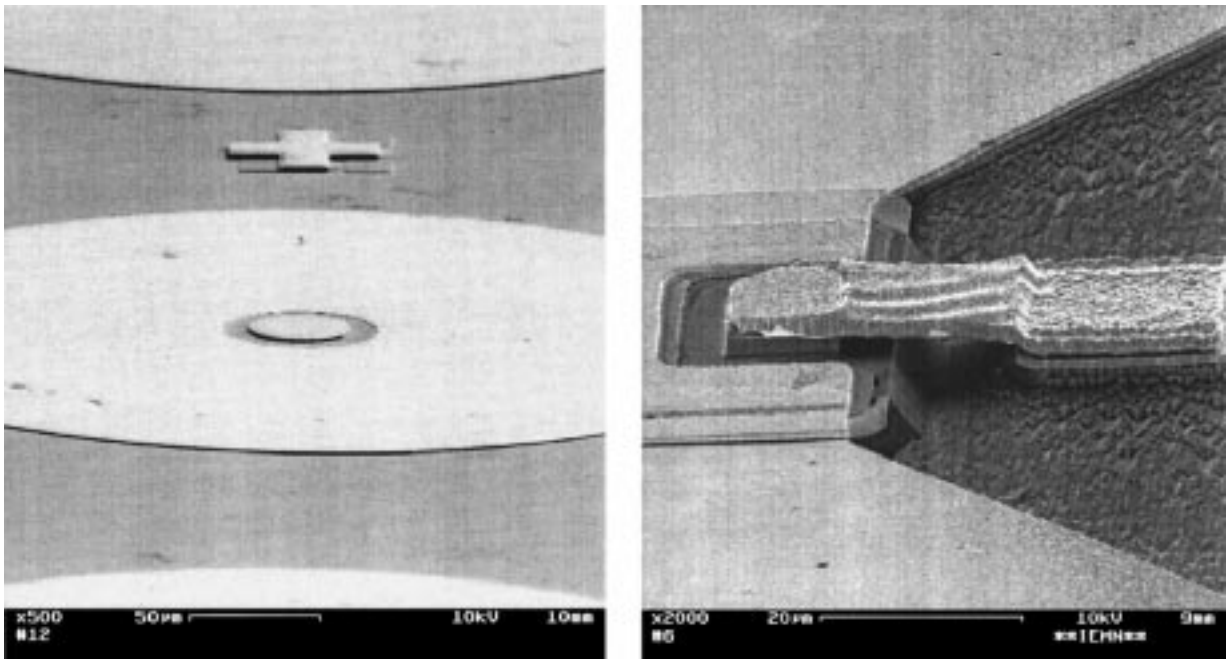


(a) (b)

Fig. 1. SEM photographs of (a) a coaxial probing pattern and (b) a CPW-type configuration with an air-bridged device. In (a) the probes are positioned directly onto the pads.

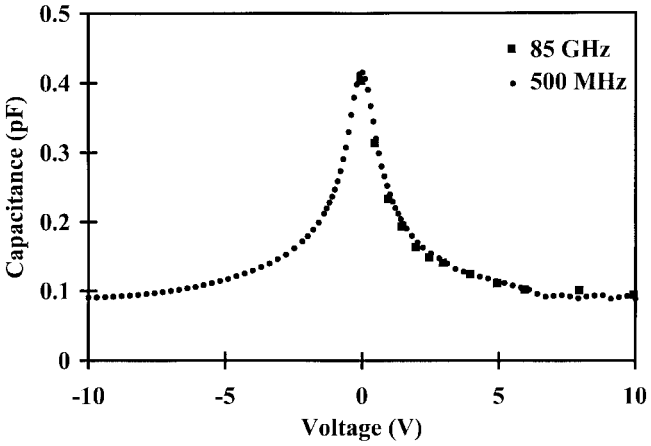


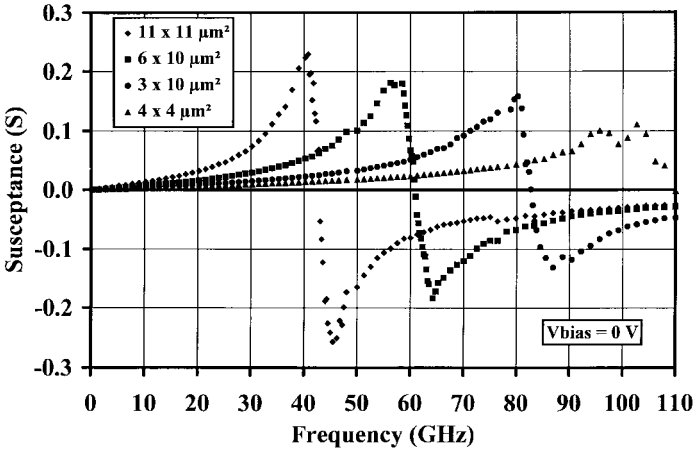
Fig. 2. *CV* characteristics measured at 500 MHz (•) and 85 GHz (■).

alyzers from 0.25 to 50 GHz, in V-band (50.0–75.0 GHz) and in W-band (75–110 GHz), respectively. TRL calibration techniques were used after positioning coplanar probes at the ends of CPW footprints. In that reference plane, the susceptance of the device here with a doping concentration of 2×10^{17} cm^{-3} shows a resonance effect which, as expected, strongly depends on the device area [Fig 3(a)]. Such a shift in the resonance frequency (f_r) can also be obtained by biasing the device. This introduces a voltage-dependent capacitance modulation with strong impact on f_r [Fig. 3(b)], notably at low voltages.

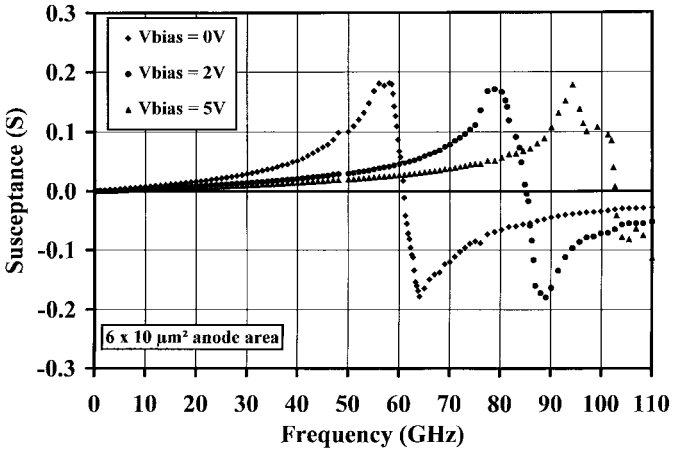
At this stage, we have two sets of experimental data which can be used for assessing the influence of the diode environment. In the past, this was often carried out by assuming a lumped equivalent circuit including both intrinsic and extrinsic elements. With the recent advances in three-dimensional electromagnetic (EM) simulations such an assumption can now be raised. In the present work, we used the procedure published in [6] for taking the active device into account in the EM simulation of the access and interconnecting regions. This method can be compared to that experimentally employed to measure the impedance "seen" by the devices on scaled prototypes of multiplier blocks. One defines two inputs ports. The first one is located at CPW access reference plane. The second one is introduced by means of a small coaxial transmission line contacting the capping and side highly doped regions (equivalent to finite conductivity metallic regions).

EM simulation was carried out with the commercial High Frequency Structure Simulator (HFSS) by HP starting from the layout displayed in the inset of Fig. 4 by a 5-GHz frequency step. The output data are the scattering parameters S_{ij} calculated between the two ports defined above. Subsequently, we calculated by means of the commercial software Microwave Design System (MDS) by HP the frequency variation of the reflection coefficient S_{11} in the CPW reference plane. The other port is loaded by a capacitance in series with a resistance whose intrinsic values correspond to those measured in a coaxial technology. The parallel conductance, reflecting the parasitic conduction through the device, was neglected owing to the extremely low leakage current of the fabricated components.

In Fig. 4, we compared the measured and calculated variations of S_{11} plotted on Smith chart for a 6×10-μm^2 unbiased device. Overall, the agreement between modeling and experiment is good. In particular the calculated resonance frequency ($f_r = 65$ GHz) fits well the measured one. The slight discrepancy in the upper limit of the frequency band



(a)



(b)

Fig. 3. Frequency dependence of the imaginary part of the diode admittance measured in a CPW configuration. The area contact or the device biasing are taken as a parameter.

can be explained by some simplifications in the device layout modeled by HFSS and by the assumption of an overall series resistance kept constant ($R_s = 2.5\ \Omega$) over the frequency band. In fact, an increase in the resistive contribution can be expected based on skin effect considerations.

By investigating the impact of the top contact geometry, it was found that the series resistance does not scale with the device area. This was interpreted by a dominant contribution of the spreading resistance to the overall resistance. This conclusion was also supported by the fact that the ohmic contact resistance measured from TLM pattern was very low ($2 \times 10^{-7}\ \Omega \cdot \mathrm{cm}^2$). Consequently, the cutoff frequency $f_c = (S_{\max} - S_{\min})/2\pi R_s$, which is a figure of merit of the device frequency capability, has to be defined for a specific planar topology. For our tripling application from 83 to ~250 GHz, harmonic balance simulations shows that the optimum area was close to 60 $\mu\mathrm{m}^2$ for an input power of about 100 mW. This means that f_c would be in excess of 2 THz in the present technology.

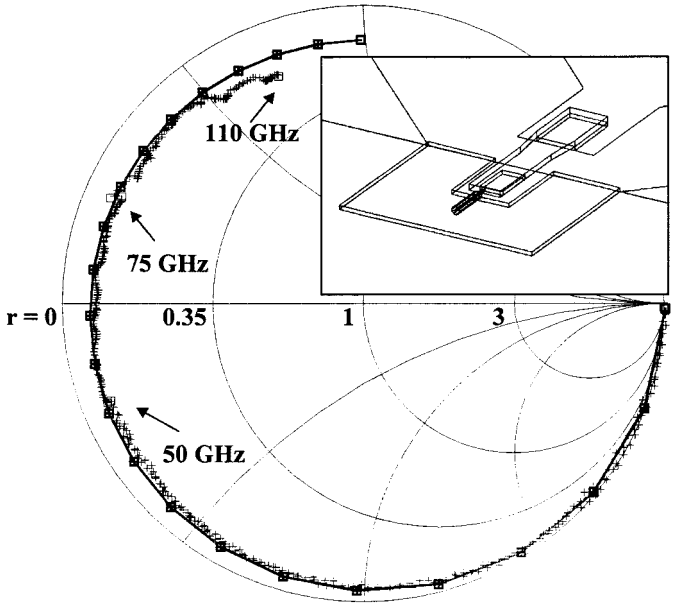


Fig. 4. Measured (+) and calculated (□) S_{11} variations versus frequency. The diode area is $6 \times 10\ \mu\mathrm{m}^2$. Inset shows the device layout simulated with HFSS with a coaxial access line to take the diode into account.

IV. Conclusion

High-quality devices InP-based HBV's have been fabricated and RF tested over a broad frequency band. The devices exhibit state-of-the-art performances in terms of capacitance characteristics and voltage handling with zero-bias capacitance as low as 1 fF/cm^2, and capacitance ratio of 5:1 with practically no deviation versus frequency. Good agreement was also found between experiment and EM simulation of reflection coefficient of the diode embedded in its environment.

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